REMARKS

Applicant appreciates the Examiner's thorough examination of the subject application and requests reconsideration of the subject application based on the foregoing amendments and the following remarks.

Claims 1-21 are pending in the subject application.

Claims 1-21 stand rejected under 35 U.S.C. §103.

35 U.S.C. §103 REJECTIONS

Claims 1-21 stand rejected under 35 U.S.C. §103 as being unpatentable over over Suzuki et al. [USP 6,445,367; "Suzuki"] in view of Hughes et al. [USP 5,920,261; Hughes] and Yoshida [USP 5,889,817; "reference"] for the reasons provided on pages 2-5 of the above-referenced Office Action. Applicant respectfully traverses as discussed below.

As grounds for the rejection the above-referenced Office Action asserts that Suzuki teaches a control circuit (103) through which an image signal enters from the outside and which generates control signals, Tscan and Tmry, that are applied to a latch circuit (105). It is further asserted that the latch circuit (105) is used as a memory circuit for storing one line of the image data for a certain period of time only. It also is asserted that Suzuki teaches a shift register that is used for converting the image data, which enters serially in a time series to parallel signals every line of the image. In this regard Applicant necessarily assumes that the Examiner is referring to the shift register identified by reference numeral 104 in figure 14 of Suzuki. Applicant respectfully disagrees with this characterization of the teachings of Suzuki.

Applicant claims, claim 1, a signal production circuit for producing a plurality of kinds of pulse signals as well as claims, claim 9, a display device including such a signal production circuit, which signal production circuit includes, *inter alia*: (1) *storage means* for storing, as digital data, a single signal of serial data including a time series of data pulses representative of all rise and fall timings of the plurality of kinds of pulse signals and data pulses representative of all time intervals between the rise and fall timings; and (2) *serial-to-parallel converter means* for reading the signal of serial data from the storage means and producing, as parallel data, the plurality of kinds of pulse signals from the data representative of all the predetermined rise and fall timings of the plurality of kinds of pulse signals. It necessarily follows from the foregoing that the storage means is operably coupled to the serial-to-parallel converter means such that the signal of serial data stored in the storage means can be read by the serial-to-parallel converter means such that the signal of serial data is converted within the converter so as to produce the plurality of parallel signals therefrom.

Reference shall be made to the attached figure 14 from Suzuki that has been annotated to further clarify the following discussion as to what is being disclosed and taught in Suzuki. Suzuki discloses and teaches a method and apparatus for driving an electron source so a high quality image can be displayed. The principal focus of this reference concerns correcting for non-uniform effective current distribution caused by the leakage current which non-uniform current distribution causes problems in the image quality (e.g., luminance).

Suzuki discloses (see col. 13, line 11 through col. 14, line 25) that a display panel 101 is connected to external electrical circuitry via terminals D_{x1} -D_{xm} and terminals D_{y1} - D_{yn}. A high-

voltage terminal Hv on a face place is connected to an external high-voltage power supply V_a and is adapted to accelerate emitted electrons. Scanning signals for successively driving, one row at a time, multiple electron beam sources provided within the panel, namely a group of surface-conduction electron emission elements matrix-wired in the form of M rows and N columns, are applied to the terminals D_{x1} - D_{xm}. Modulating signals for controlling the output electron beams of the respective elements of the surface-conduction electron emission elements in a row selected by the scanning signals are applied to the terminals D_{y1} - D_{yn}.

The scanning circuit 102 in Suzuki is internally provided with M-number of switching elements. On the basis of a control signal Tscan issued by a control circuit 103, each switching element connects a DC power supply V_{x1} to the wiring terminal of a row of electron elements being scanned and a DC power supply V_{x2} to the terminal of a row of electron emission elements not being scanned.

Suzuki further indicates that on the basis of an image signal that enters from the outside, the control circuit 103 acts to coordinate the operation timing of each component so as to present an appropriate display. The externally applied image signal may be a composite of image data and a synchronizing signal, as in the manner of an NTSC signal, or it may be an image signal in which the image data and synchronizing signal are separated in advance. As to the discussion regarding figure 14, Suzuki indicates that the device of figure 14 is being described in the case in which the image data and synchronizing signal are separated in advance.

In Suzuki, the control circuit 103 generates control signals Tscan and Tmry that are applied to the scanning circuit 102 and a latch circuit 105, respectively, on the basis of an

externally entered synchronizing signal Tsync. The synchronizing signal Tsync generally comprises a vertical synchronizing signal and a horizontal synchronizing signal but is designated by Tsync in Suzuki in order to simplify the description.

In use, the externally applied image data 5000 (luminance data) enters a shift register 104 and the shift register 104 is for converting the image data, which enters serially in a time series, to a parallel signal every line of the image. The shift register 104 operates based upon the control signal (shift clock) Tsft which enters from the control circuit 103.

The serial/parallel-converted data of one line of the image (which data corresponds to the drive data of N-number of electron emission elements) is outputted from the shift register 104 to the latch circuit 105 as parallel signals I_{d1} - I_{dn}. The latch circuit 105 is a memory circuit for storing one line of the image data for a requisite period of time only. More particularly, in Suzuki the latch circuit 105 stores the output signals from the shift register, namely I_{d1} - I_{dn}, simultaneously in accordance with the control signal Tmry sent from the control circuit 103. The data stored in the latch circuit 105 is in turn outputted to a voltage modulating circuit 106 as I'_{d1} - I'_{dn}.

The voltage modulating circuit 106 produces a voltage signal, the amplitude of which has been modulated in dependence upon the image data I'_{d1} - I'_{dn} and outputs the voltage signal as I''_{d1} - I''_{dn} (the greater the luminance of the image data, the larger is the amplitude of the voltage that is outputted). The output signals I''_{d1} - I''_{dn} from the voltage modulating circuit 106 enter a voltage/current converting circuit 107. The voltage/current converting circuit 107 is a circuit for controlling the current that is passed through the cold cathode element in dependence upon the

amplitude of the input voltage signal. The output signal of the voltage/current converting circuit 107 is applied to terminals D_{y1} - D_{yn} of the display panel 101.

As indicated above, the signal production circuit of claims 1 or 9 includes, *inter alia*: (1) *storage means* for storing, as digital data, a single signal of serial data including a time series of data pulses representative of all rise and fall timings of the plurality of kinds of pulse signals and data pulses representative of all time intervals between the rise and fall timings; and (2) *serial-to-parallel converter means* that *inter alia* reads the signal of serial data from the storage means. It is clear form the above discussion provided in Suzuki, that the shift register 104 in Suzuki is being equated to the serial-to parallel converter means of the present invention and that the latch circuit 105 is being equated to the storage means of the present invention. It can be seen, however, that these features in Suzuki do not correspond to the allegedly corresponding features of the present invention and moreover, these features are not arranged in the manner as set forth in claim 1.

As set forth in claims 1 and 9, the storage means stores a single signal of serial data including a time series of data pulses representative of all rise and fall timings of the plurality of kinds of pulse signals and data pulses representative of all time intervals between the rise and fall timings. In contrast, in Suzuki the latch circuit 105 stores the parallel-converted data of one line of the image (which data corresponds to the drive data of N-number of electron emission elements) being *outputted from* the shift register 104.

It also is thus clear that the above described circuit arrangement in Suzuki cannot disclose or teach as is claimed by Applicant a serial to parallel converting means for *reading a signal of*

serial data from the storage means. It is clear that in Suzuki the serial data is external to the electron-beam generating device/ apparatus and is inputted directly to the shift register 104 from the outside. As such, it is physically impossible for the shift register 104 in Suzuki to read serial data from the latch means 105 because in Suzuki the shift register 104 and the latch means 105 are arranged so the shift register outputs parallel data to the latch means.

The above-referenced Office Action further asserts that Suzuki teaches a pulse width modulating circuit (7111), a correction circuit (7489) and LUT (7108) that stores leakage currents as well as applied voltage waveforms plots with respect to power supply and emission current. Applicant would note that the LUT is mischaracterized in that, what is stored in the LUT is not leakage currents but rather there is stored in the LUT n -number of leakage resistances (Rleak(N)) at corresponding addresses of the 1 x n addressed provided in the LUT (see col. 40, lines 25-45). As to the pulse-width modulating circuit 7111, Suzuki indicates that circuit element generates drive pulses having a pulse width that corresponds to the video signal intensity.

The above-reference Office Action acknowledges that Suzuki does not teach serial to parallel converting means for reading a signal of serial data from storage means and producing as parallel data such that data from the storage means includes digital data including all pulses representative of all rise and fall timings. It is asserted, however, that Hughes teaches a technique of Manchester phase encoding. It is further indicated that in view of the suggestion in Hughes, the Manchester encoding techniques as shown in figures 2 and 6 of Hughes equivalently

provides the desired single signal incorporating the time series of data pulses. Applicant respectfully disagrees with the characterization of what is being taught or described in Hughes.

As indicated in Hughes (see col. 4, lines 50-55), the technique shown in figure 2 thereof is the well-known Manchester phase encoding technique or split-phase encoding technique. As is known to those skilled in the art, Manchester encoding or Manchester phase encoding is a synchronous clock encoding technique to encode the clock and data. In telecommunications, which is the art described in Hughes, Manchester encoding is a form of data communication in which each bit of data being transmitted is signified by at least one transition. As such, Manchester encoding is considered to be self-clocking, which means that synchronization of the data stream is possible.

In this technique, each bit period is split into two, and a transition between signal levels representative of a logic state (*e.g.*, 1 to 0) is made to occur in the middle of each bit of a synchronous bit stream. There are two opposing conventions for the representation of the data. In one of these convention, which also is described in Hughes, for logic 1 bit signals, the signal levels during a bit period will be high to low, namely the signal will be at a high level in the first half of the bit period and at a low level in the second half of the bit period. Similarly, for a logic 0 bit signal, the signal levels during a bit period will be low to high, namely the signal will be at a low level in the first half of the bit period and at a high level in the second half of the bit period. The other convention (*e.g.*, see IEEE 802.4 standard) is that a logic 0 bit is represented by a high to low signal sequence and a logic 1 bit is represented by a low-high sequence. Applicant

encloses herewith some definitional materials obtained from an Internet search further describing Manchester encoding.

In sum, the Manchester encoding technique does not change the form of the data stream so as to be a single signal of serial data as is set forth in the claims as well as the subject application. Rather it is a data encoding technique whereby a parallel data stream is reformatted so as to produce another parallel data stream having a different bit rate (double the bit rate of the first data stream). As such, Applicant respectfully submits that the use of the Manchester encoding technique as shown and taught in Hughes would **not** equivalently provide the desired single signal incorporating the time series of data pulses.

In the Manchester Phase Encoding as taught in Hughes for example, a clock can be generated from data, however, as with the foregoing method, the number of data still remains the same even after the conversion. More specifically, in the event where 4 x 4 = 16 data are required, the signal production circuit of the present invention initially requires only four serial data, as illustrated in Fig. XB attached hereto below. In contrast, in common serial-to-parallel conversion, sixteen serial data are initially required because the conversion merely rearranges the data or changes the bit rate of data as is illustrated in Fig. XA attached hereto.

Applicant would note that the foregoing should not be interpreted as or be understood to be a waiver of any argument as to the appropriateness of the suggested combination of Suzuki and the teachings of Hughes *ab initio*. Applicant believes that Examiner has not provide a sufficient basis as to why one skilled in the art of designing circuits for display apparatuses would have been motivated to use a technique for sequencing or synchronizing data being

transferred between a transmitter and a corresponding receiver in a circuit design and method in the processing and displaying image data arts.

It also is acknowledged in the Office Action (*e.g.*, see page 3 thereof) that Suzuki does not teach serial to parallel converter means for reading a signal of serial data from the storage means and producing parallel data.[1] It is asserted in the Office Action, however, that Yoshida teaches a 16 bit shift register (1012) that is provided between a Manchester decoding circuit (1010) and a serial/ parallel conversion circuit (1011). It is concluded that it would have been obvious to one skilled in the art at the time the invention was made to modify the image forming apparatus disclosed in Suzuki to include Yoshida's use of serial/ parallel conversion circuit 1010). The asserted motivation being that one would have been motivated in view of the suggestion in Yoshida that the serial/ parallel circuit (1011) along with the Manchester decoding circuit 1010 as configured in Fig. 1 equivalently provides the desired serial-to-parallel converter means. There also appears to be an assertion that the use of such a circuit helps function a communication system including displays as taught by Yoshida.

Yoshida describes the serial/ parallel conversion circuit 1011 in column 1, line 61 - column 2, line 60. As described therein, the input data to the serial/parallel conversion circuit 1011 is the serial data of individual 8-bit data D1-D7, as illustrated in Fig. 11 and Fig. 12 of Yoshida. In Yoshida, the serial data is decoded by the Manchester decoding circuit 1010, delayed by the 16-bit shift register 1012, and inputted to the serial/parallel conversion circuit 1011. The serial/parallel conversion circuit 1011 converts the serial 8-bit data D1-D7 into

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[1] This assertion is inconsistent with the discussion on page 2 of the Office Action. This also amounts to an

parallel data, and supplies the parallel data to the receive FIFO 1007. That is, the serial/ parallel conversion circuit 1011 in Yoshida merely reconverts the serial 8-bit data D1-D7 into parallel data.

In contrast, the serial-to-parallel converter means of the present invention reads serial data contained in the storage means, and generates parallel pulse signals of different kinds based on the rise and fall timings of the serial data. That is, the function of the serial-to-parallel converter means of the present invention is not merely to rearrange data but to generate pulse signals based on the rise and fall timings of serial data. Thus, in this respect, the serial-to-parallel converter means of the present invention is clearly different, both structurally and functionally, from the serial/ parallel conversion circuit 1011 of Yoshida.

Even assuming that the foregoing features in Yoshida taught the claimed serial-to-parallel conversion means, which it does not, this still does not mean that the suggested combination would yield the claimed invention. As indicated above, the serial data (digital video signal or luminance data 5000) in Suzuki is externally applied to the shift register 104 and the parallel data outputted therefrom is inputted to the latch circuit 105, which apparently is asserted to correspond to the storage means of the present invention. Thus, and what the cited art totally lacks is any teaching or motivation for locating a serial-to-parallel converter means between the latch circuit 105 and the voltage modulating circuit 106 of Suzuki. The lack of such a motivation is not surprising because such a modification would completely destroy the intended purpose, function and operation of the electron-beam generating device disclosed in Suzuki.

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admission that Suzuki is lacking all of the features as set forth in claims 1 or 9.

This assertion also appears to be predicated on the fact that the Manchester encoding technique would equivalently provide the desired single signal incorporating the time series of data pulses. As indicated above, the Manchester encoding technique does not change the form of the parallel data stream so as to be a signal of serial data as is set forth in the claims as well as the subject application. Rather it is a data encoding technique whereby a parallel data stream is reformatted so as to produce another parallel data stream having a different bit rate from the first data stream (*i.e.*, double the bit rate of the first data stream). As such, it necessarily follows that the use of the Manchester encoding technique in Yoshida also would **not** equivalently provide the desired single signal incorporating the time series of data pulses. It necessarily follows that the allegedly corresponding features in Yoshida cannot correspond to the desired serial-to parallel converter of the claimed invention because of this.

Applicant would note that the foregoing should not be interpreted as or be understood to be a waiver of any argument as to the appropriateness of the suggested combination of Suzuki and the teachings of Hughes and Yoshida. Applicant believes that Examiner has not provide a sufficient basis as to why one skilled in the art of designing circuits for display apparatuses would have been motivated to use techniques for sequencing or synchronizing data being transferred between a transmitter and a corresponding receiver (*i.e.*, the telecommunication arts) in a circuit design and method in the processing and displaying image data art.

As to claim 2, this claim include the further limitation that the serial-to-parallel converter means includes a plurality of flip-flops, connected in cascade so that an output signal of one flip-flop is an input signal of a next, which convert data from serial to parallel by sequentially

latching input data based on the signal of serial data which serves as a common clock signal to all the flip-flops, and that the so-configured serial-to-parallel converter means derives output signals from predetermined ones of the plurality of flip-flops as the parallel data. The lines referred to in the Office Action do not describe the use of flip-flops as a serial-to-parallel converter means and more specifically, there is no mention anywhere in Suzuki of a converter means as described in claim 2 that also derives output signals from predetermined ones of the plurality of flip-flops as the parallel data. It is respectfully submitted that the forgoing comments as to claim 2 also applies to distinguish claim 3 from the cited combination of references.

As to claim 4, this claims includes the further limitation that the signal production circuit further includes a control switching means for supplying the produced plurality of kinds of pulse signals to a plurality of circuits which operate in respective sequences of a common frame period, by switching from one circuit to another at the common frame period. In support of this rejection, reference is made to the scanning circuit 4102 in Suzuki. Applicant would note that while the circuitry illustrated in figure 22 of Suzuki includes a scanning circuit, the circuitry does not show, describe nor teach how the plurality of kinds of pulse signals produced by the serial-to-parallel converter means are supplied to a plurality of circuits by the scanning circuit.

As to claim 5, this claim further provides that the serial-to-parallel converter means performs an AND operation between the signal of serial data and data pulses with a pulse period equal to, or shorter than, a base pulse width of the signal of serial data and with a base pulse width 1/n times that of the signal of serial data, where n is an integer, before the conversion to the parallel data is performed. This assertion that that which is shown in figure 19 and 20 of Suzuki

describe or teach the production circuit as set forth in claim 5 does not agree with the discussion in col. 35, lines 31-95 of Suzuki regarding the waveforms shown in figures 20A-C. It is clear from the discussion therein that the waveform in figure 20A correspond to the waveforms from the pulse-width modulating circuit 206 that processes the parallel data from the latch circuit/ latch means 205. Thus, it can hardly be said that this circuit element (pulse-width modulating circuit 206) teaches a feature of the serial-to-parallel converter means of the present invention.

As to claim 6, Applicant would note that Suzuki nowhere describes, teaches or suggests that serial-to-parallel converter means decomposes the single signal of serial data into signals of serial data, each of these serial signals being representative of one of a plurality of sequences, and then produces the parallel data from the so signals of serial data resulting from the decomposing process. As indicated above, the serial data in Suzuki is externally applied to the shift register 104 and that the data outputted from the shift register is parallel data.

As to claim 14, this claims provides that one of the plurality of pulse signals produced by the serial-to-parallel converter means is overlapped in time with another of the plurality of pulse signals produced by the serial-to-parallel converter means. Notwithstanding what is asserted in the Office Action as being taught in Hughes, the electron beam generating device in Suzuki could not generate a display if one of the plurality of signals from the shift register overlapped in time with another of the plurality of pulse signals from the shift register. Basically, the serial data signals in Suzuki cannot overlap each other in time otherwise one could not produce a display of the image data being transmitted. As such, there can be no motivation to combine since the suggested combination would destroy the functionality of the device disclosed in Suzuki. The

foregoing remarks regarding claim 14 also apply to distinguish claims 15, 18 and 19 from the cited combination of references.

As to claim 16, this claim further provides that the plurality of kinds of signals being produced by the serial-to-parallel converter means are control signals for controlling a device embodying the signal production circuit. Applicant respectfully submits that whatever Hughes allegedly teaches, the allegedly corresponding elements to the present invention in Suzuki do not output control signals that control the beam-generating device disclosed in Suzuki. Moreover, there is no teaching or suggestion anywhere in Suzuki or the other cited references to configure the control circuit 103 disclosed in Suzuki so as to be capable of outputting control signals using the signal production circuit claimed by Applicant. The foregoing remarks regarding claim 16, also apply to distinguish claim 17 from the cited combination.

As to claims 20 and 21, Applicant claims, claim 20, a signal production circuit for producing a plurality of kinds of pulse signals as well as claims, claim 21, a display device including such a signal production circuit, which signal production circuit includes, *inter alia*: (1) a *memory* for storing, as digital data, a single signal of serial data including a time series of data pulses representative of all rise and fall timings of the plurality of kinds of pulse signals and data pulses representative of all time intervals between the rise and fall timings; and (2) *serial-to-parallel converter means* for reading the signal of serial data from the storage means and producing, as parallel data, the plurality of kinds of pulse signals from the data representative of all the predetermined rise and fall timings of the plurality of kinds of pulse signals. It necessarily follows from the foregoing that the memory is operably coupled to the serial-to-parallel converter

means such that the signal of serial data stored in the storage means can be read by the serial-to-parallel converter means such that the signal of serial data is converted within the converter so as to produce the plurality of parallel signals therefrom. Applicant respectfully submits that the foregoing remarks distinguishing the signal production circuit of claim 1 and the display device of claim 9 from the cited combination of references also apply to distinguish the signal production circuit of independent claim 20 and the display device of independent claim 21 from the same cited combination of references.

It is respectfully submitted that the foregoing remarks regarding claims 1 and 9 also apply to distinguish each of claim 7, 8, and 10-13 from the combination or references.

As provided in MPEP 2143.01, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. *In re Fine*, 837 F. 2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F. 2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). As provided above, the references cited, alone or in combination, include no such teaching, suggestion or motivation.

Furthermore, and as provided in MPEP 2143.02, a prior art reference can be combined or modified to reject claims as obvious as long as there is a reasonable expectation of success. *In re Merck & Co., Inc.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 19866). Additionally, it also has been held that if the proposed modification or combination would change the principle of operation of the prior art invention being modified, then the teachings of the references are not

sufficient to render the claims *prima facie* obvious. Further, and as provided in MPEP-2143, the teaching or suggestion to make the claimed combination and the reasonable suggestion of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). As can be seen from the forgoing discussion regarding the disclosures of the cited references, there is no reasonable expectation of success provided in the references. Also, it is clear from the foregoing discussion that the modification suggested by the Examiner would change the principle of operation of the circuitry disclosed in Suzuki.

The Federal Circuit has indicated in connection with 35 U.S.C. §102 that in deciding the issue of anticipation, the trier of fact must identify the elements of the claims, determine their meaning in light of the specification and prosecution history, and identify *corresponding elements* disclosed in the allegedly anticipating reference (emphasis added, citations in support omitted). *Lindemann Maschinenfabrik GMBM v. American Hoist and Derrick Company et al.*, 730 F. 2d 1452, 221 USPQ 481,485 (Fed. Cir. 1984). Notwithstanding that the instant rejection is under 35 U.S.C. §103, in the present case the Examiner has not shown that the shift register, the latch circuit and the arrangement of these elements in Suzuki, alone or in combination with the other cited art, corresponds, as that term is used above by the Federal Circuit, in any fashion to the storage means, the serial-to-parallel converter means and the arrangement of the storage means and the serial-to-parallel converter means in its entire claimed form as set forth in any of the independent claims of the present invention.

As provided by the Federal circuit, a 35 U.S.C. §103 rejection based upon a modification of a reference that destroys the intent, purpose or function of the invention disclosed in a

reference, is not proper and the prima facie case of obviousness cannot be properly made. In short there would be no technological motivation for engaging in the modification or change. To the contrary, there would be a disincentive. *In re Gordon*, 733 F. 2d 900, 221 USPQ 1125 (Fed. Cir. 1984). In the present case it is clear that if electron beam generating device/ apparatus disclosed in Suzuki was modified in the manner suggested by the Examiner, as well as that allegedly taught in either of Hughes or Yoshida, it would destroy the intent, purpose or function of the device as taught by Suzuki.

Although a prior art device "may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so." *In re Mills*, 916 F. 2d, 680, 682; 16 USPQ 2d 1430, 1432 (Fed. Cir. 1990). See also *In re Fritch*, 972 F. 2d 1260, 23 USPQ 2d 1780 (Fed. Cir. 1992).

As the USPTO Board of Patent Appeals and Interferences has held, "The mere fact that a worker in the art could rearrange the parts of the reference device to meet the terms of the claims on appeal is not by itself sufficient to support a finding of obviousness. The prior art must provide a motivation or reason for the worker in the art, without benefit of appellant 's specification, to make the necessary changes in the reference device." *Ex parte Chicago Rawhide Mfg. Co.*, 223 USPQ351, 353 (BD. Pat. App. & Inter. 1984).

In one case, claims to a hydraulic press which read on the prior art except with respect to the position of the starting switch were held unpatentable because shifting the position of the starting switch would not have modified the operation of the device. *In re Japikse*, 181 F. 2d 1019, 86 USPQ 70 (CCPA 1975). It also was held that the particular placement of a contact of a

conductivity measurement device was an obvious matter of design choice because, *inter alia*, the particular placement of the contact provides no novel or unexpected result. *In re Kuhle*, 526 F. 2d 553, 188 USPQ 7 (CCPA 1975). However, it is clear from the foregoing remarks that the suggested modification to the electron beam generating device disclosed in Suzuki would require a modification to the operation of the disclosed device and/or is more than an obvious matter of design choice.

As the Federal circuit has stated, "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." *In re Fritch*, 972 F.2d 1260,1266, 23 USPQ2d 1780, 1783-84 (Fed. Cir. 1992). Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor. *Para-Ordance Mfg. v. SGS Importers Int'l, Inc.*, 73 F.2d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995).

It is respectfully submitted that for the foregoing reasons, claims 1-21 are patentable over the cited reference(s) and thus, satisfy the requirements of 35 U.S.C. §103. As such, these claims are allowable.

OTHER MATTERS

Applicant filed a Supplemental Information Disclosure Statement/ Search Report Information Disclosure Statement dated December 22, 2003, which IDS post-dates the above-referenced Office Action. Accordingly, Applicant respectfully requests that the Examiner reflect their consideration of this IDS in the next official communication from the USPTO. Applicant also

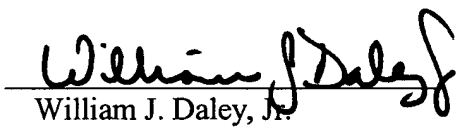
respectfully requests the Examiner to call the undersigned collect and the below number in the event that this IDS has not been received by the Examiner and thus needs to be again submitted by Applicant for the Examiner's consideration.

It is respectfully submitted that the subject application is in a condition for allowance. Early and favorable action is requested.

Applicant believes that additional fees are not required for consideration of the within Response. However, if for any reason a fee is required, a fee paid is inadequate or credit is owed for any excess fee paid, the Commissioner is hereby authorized and requested to charge Deposit Account No. **04-1105**.

Respectfully submitted,
Edwards & Angell, LLP

Date: January 26, 2004

By: 

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